IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	May 13, 2009
Kubo, et al	Group Art Unit: 2621
Serial No. 10/716,791	Examiner: David Werner
Filed: November 19, 2003	IBM Corporation Anne Vachon Dougherty 3173 Cedar Road Yorktown Hts, NY 10598
Title: FORMAT CONVERSION CIRCUIT	

Board of Patent Appeals and Interferences
Alexandria, VA 22313-1450

REPLY BRIEF

The remarks which follow are submitted in response to the present Examiner's Answer dated April 14, 2009, in the above-identified application. The arguments presented by Applicants (hereinafter "Appellants") in the Appeal Brief dated January 14, 2009, are hereby incorporated by reference herein.

Appellants will respond herein to certain arguments raised by the Examiner in the **(10) Response to Argument** section of the Examiner's Answer (hereinafter "Answer").

XI. RETORT TO EXAMINER'S RESPONSE TO ARGUMENT

Claims 1, 6, 7

Appellants disagree with the Examiner's interpretation of the earlier-presented arguments. The Examiner breaks the arguments into "three specific alleged faults".

With respect to the Settle patent, the Examiner concludes that Appellants only argument is "the alleged failure of the Settle reference to produce packets including a 'packet header' and 'a predetermined amount of video data'".

In fact, Appellants acknowledged that generating packet headers and packets with headers and payload is known (see: Appeal Brief, page 9). Settle teaches that headers are added (at both packetizers 18a and 18b of Fig. 2) to produce packets (produced by encoders 12 and 14) and that the packets with headers are multiplexed by Unit 20 (see: Col. 4, lines 31-57). Settle neither teaches nor suggests alternately repeatedly the selection of a packet header and the selection of a predetermined amount of packet payload in real time during an interval between detection of a synchronization signal for the line of data and detection of

a synchronization signal for a successive line of data. By storing the unpacketized data and reading it out in real time alternately with header information, the present invention not only achieves real-time conversion of the data using the horizontal synchronization period, but also does so without having to store all of the input data in capture circuitry (see: Specification, page 1, line 25-page 2, line 7 and page 15, line 26-page 16, line 4). Like the prior systems noted in the Background section of the present application, Settle requires a capture circuit (computer memory 108 of Figs. 6 and 8, see: Col. 10, lines 38-46) which stores **all** of the input data packets, from which Settle retrieves the stored packets and provides them to the Fig. 2 circuitry to produce its MPEG "compatible" packets. Even if Settle is found to teach generating header and payload for MPEG transport packets, Settle does not teach or suggest the real-time format conversion system and method with alternate selection of header and payload data in real time during a period between detection of a first and a successive synchronization signal.

With regard to Tsubouchi, the Examiner summarizes Appellants' arguments as "the alleged failure of the Tsubouchi et al. to disclose the claims 'synchronous timing

detector' or 'synchronous timing detecting device'." However, the Examiner's comments on page 10 say 'applicant states that the data bus cited in the Final rejection as delivering the claimed 'synchronizing signal' does not necessarily operate on 'digitized' data as required by the preamble of claim 1, and so is not applicable to the present invention".

Again, Appellants respectfully assert that the Examiner has not appropriately characterized Appellants' arguments. Appellants argued that, even if one combines Settle and Tsubouchi, such that Settle would send packets in response to a Tsubouchi signal, the combination would not obviate the invention as claimed, since the combination of Settle and Tsubouchi does not teach or suggest the claimed packetizing (i.e., repeating the alternate selecting of a packet header and then selecting a predetermined amount of video data as payload in real time) of digitized data. Settle teaches that headers are added (at packetizers 18a and 18b of Fig. 2) to produced packets (produced by encoders 12 and 14) and that the packets are multiplexed by Unit 20 (see: Col. 4, lines 31-57) but does not teach or suggest repeatedly selecting a packet header and a predetermined amount of packet payload in real time. Tsubouchi teaches

that video data can be read out of a buffer in response to a signal. Modifying Settle to use a Tsubouchi signal to trigger the packetizers to generate packets would not result in the claimed packetizing comprising repeating the alternate selecting of a packet header and then selecting a predetermined amount of video data as payload in real time during a time between detection of a first synchronizing signal and a next synchronizing signal.

The Examiner acknowledged that "the combination of Settle et al alone (sic) and Tsubouchi et al. the (sic) enable pulse in Tsubouchi et al. for reading video data from a buffer is not a horizontal synchronization signal, operating on digitized video data comprising a plurality of data lines, each followed by a horizontal synchronization period".

In the Answer, the Examiner concluded that "Appellant states that Yamauchi describes a system in which a reading operation from a data buffer is controlled exclusively with a signal based on a vertical synchronization period of a video" but that "Appellant does not consider the write signal, described in the Yamauchi et al. reference as controlled by the horizontal synchronization period, to be relevant." Appellants acknowledged that Yamauchi teaches

writing video data into memory using Sf1, a horizontal reference signal for counting samples 123 to 842. The Examiner states that "Yamauchi et al. was cited to demonstrate that it was known in the art to use the horizontal synchronization of a raster video signal to perform control operations of a buffer...". But the pending claims do not recite use of a horizontal synchronization signal to control buffer operations. The claims recite steps and means for detecting a synchronizing signal and then steps and means for alternately selecting header data and payload data during the interval from the detected synchronizing signal to the next detected synchronizing signal. The selecting signal is not the detected synchronizing signal (see: Fig. 9 showing both a horizontal synchronous signal and a select signal). Moreover, the detected synchronizing signal is not the horizontal synchronization period. The horizontal synchronization period is, as detailed in the Specification on page 9, lines 24-29, a period existing between lines during which no valid video data exists. The present invention uses that "dataless" period before the next detected synchronizing signal to complete the real-time selecting/reading out of the rest of the payload for the line (see: Specification at

page 10, lines 10-14 and page 16, lines 21-25). Clearly the Examiner's conclusion that it would be obvious to use Yamauchi's teachings "with the result of not digitizing or transmitting non-video data presented during the horizontal control period" are inconsistent with the teachings and claims of the present application wherein the data is selected for transmission during the horizontal control period.

Claim 2

Appellants rely on the arguments set forth previously with respect to Claim 2.

Claim 3

Appellants rely on the arguments set forth previously with respect to Claim 3.

Claims 4-5

In response to the arguments in support of Claims 4 and 5, the Examiner reiterates that the combination of Tsubouchi and Yamauchi "is not to bodily incorporate the read signal determined from a vertical synchronization of Yamauchi et

al. into the buffer of Tsubouchi, but merely that is was known in the art to control the timing of a buffer operation based on horizontal synchronization". Appellants understand the Examiner's argument, but maintain that any combination of the teachings of the references still falls short of obviating the claim language since none of the references teaches or suggests modifying the Settle system as suggested by the Examiner. It is clearly established under U.S. Patent Law that the cited reference must provide the suggestion or motivation to combine the references and that one cannot use the teachings of the presently-pending application to supply the motivation. See *In re Vaeck,* 947 F. 2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991). Such a usage of 20:20 hindsight is an inappropriate application of the obviousness doctrine.

Moreover, even if one were motivated to modify Settle with Tsubouchi and Yamauchi, the combination would not obviate the claimed invention since none of the references teaches or claims repeating the alternate selecting of a packet header and then selecting a predetermined amount of video data as payload in real time during a time between detection of a first synchronizing signal and a next

synchronizing signal whereby the selection of video data is completed during the horizontal synchronization period.

CONCLUSION

Appellants respectfully maintain the assertion that the Examiner has erred in rejecting Claims 1-7 as unpatentable over Settle in view of Tsubouchi and Yamauchi. Appellants request that the decisions of the Examiner be overturned by the Board and that the claims be passed to issuance.

Respectfully submitted,

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